Remarks

In the Office Action mailed February 12, 2007, the Examiner rejected claims 1-19 under 35 U.S.C. § 103(a). Applicants respectfully traverse the rejections and request reconsideration.

I. Response to the Rejections under 35 U.S.C. § 103(a) Based on Librizzi/Shirato

The Examiner rejected claims 1, 2, 5, 6, 9, 10, 13, 14, and 17 under 35 U.S.C. § 103(a) as being obvious in view of the combination of U.S. Patent No. 6,429,502 ("Librizzi") and Japanese Publication No. 02271567 ("Shirato"). In claim 1, Applicants recite an integrated circuit having a semiconductor substrate, a buried insulation layer directly over the semiconductor substrate, a semiconductor mesa over the buried insulation layer, and a guard ring substantially surrounding the semiconductor mesa. The guard ring extends through the buried insulation layer contacting the semiconductor substrate.

Neither Librizzi, nor Shirato teach an integrated circuit having a guard ring as claimed. The Examiner stated, and Applicants agree, that Librizzi fails to disclose a guard ring that extends through the buried insulation layer contacting the semiconductor substrate. (Office Action, page 2.) While Shirato describes a guard ring that contacts the semiconductor substrate, Shirato's guard ring does not extend through a buried insulation layer directly over the semiconductor substrate. Instead, Shirato describes an impurity region 2 located between an insulating film 3 and a first semiconductor substrate 1. (See, e.g., Shirato, Abstract.) Thus, Shirato's guard ring extends though the insulating film 3 and the impurity region 2 to contact the semiconductor substrate.

The Examiner stated that it would have been obvious for one skilled in the art "to modify the semiconductor of Librizzi to include a guard ring that extends through the buried insulation layer

McDonnell Boehnen Hulbert & Berghoff LLP
300 South Wacker Drive
Chicago, IL 60606
Telephone: (312) 913-0001

contacting the semiconductor substrate as disclosed in Shirato because it aids in providing high integration." (Office Action, page 3.) Applicants respectfully disagree with this statement.

One skilled in the art would not modify Librizzi to include a guard ring that extends through the buried insulation layer contacting the semiconductor substrate as Librizzi specifically teaches away from the guard ring extending through the buried oxide layer. Librizzi's guard rings do not extend through the buried oxide layer (insulating layer 42) as Librizzi uses SOI technology as a source of RF isolation; specifically, the insulating layer "provides additional RF isolation." (Librizzi, col. 5, lines 60-62.)

> The first guard ring region 36 is completely isolated by the trenches 24 and 26 and the insulating layer 42. Similarly, the second guard ring region 38 is completely isolated by the trenches 30 and 32 and the insulating layer 42. This allows for easy bias of the first and second guard ring regions 36 and 38.

(Librizzi, col. 6, lines 1-6.) If Librizzi's guard rings extended through the buried oxide layer, the rings would not be completely isolated as taught by Librizzi.

Moreover, Librizzi would not be motivated by the "high integration" provided by Shirato because Shirato's high integration occurs as a result of forming capacitors on a separate substrate.

> In addition, because the capacitors required by the analog circuit configuration are formed on a separate substrate, and also are formed below the transistors, resistors etc., it is possible to achieve high integration.

(See, Translation of Shirato provided in the Response faxed November 16, 2006, page 5.) Shirato's impurity region 2 is used to form capacitors with the first semiconductor substrate 1. (See, e.g., Translation, page 6.) Thus, Applicants submit that one skilled in the art would not modify the semiconductor of Librizzi to include a guard ring that extends through the buried insulation layer contacting the semiconductor substrate as disclosed in Shirato.

Further, Shirato does not suggest forming the buried insulation layer directly over the semiconductor substrate as the impurity region is necessary in Shirato's design to form capacitors on a separate substrate. The Examiner agreed and stated that "Shirato is not utilized to disclose a buried insulation layer directly over the semiconductor substrate." (Office Action, page 5.) Thus, Applicants submit that one skilled in the art would not modify the semiconductor of Shirato to eliminate the impurity region, which is not used in Librizzi's semiconductor design.

Because neither Librizzi nor Shirato show or suggest a guard ring that extends through the buried insulation layer directly over the semiconductor substrate, Applicants submit that claim 1 is not obvious in view of the combination of Librizzi and Shirato. Claims 2, 5, 6, 9, 10, 13, 14, and 17 depend from claim 1. Accordingly, Applicants also submit that claims 2, 5, 6, 9, 10, 13, 14, and 17 are not obvious in view of the combination of Librizzi and Shirato for at least the reasons described above with reference to claim 1.

In light of the above, Applicants respectfully request withdrawal of these rejections under 35 U.S.C. § 103(a).

II. Response to the Rejections under 35 U.S.C. § 103(a) Based on Librizzi/Shirato/Beyer

The Examiner rejected claims 3, 4, 7, 8, 11, 12, 15, and 16 under 35 U.S.C. § 103(a) as being obvious in view of the combination of Librizzi, Shirato, and U.S. Patent No. 5,264,387 ("Beyer"). Claims 3, 4, 7, 8, 11, 12, 15, and 16 depend from claim 1. As described above, neither Librizzi nor Shirato show or suggest a guard ring that extends through the buried insulation layer directly over the semiconductor substrate. The Examiner cited to Beyer for the teaching of a

semiconductor device that has a semiconductor mesa that comprises a silicon mesa. (Office Action, page 4.) However, this teaching of Beyer does not overcome the deficiencies identified with respect to Librizzi and Shirato. Accordingly, Applicants submit that claims 3, 4, 7, 8, 11, 12, 15, and 16 are not obvious in light of the combination of Librizzi, Shirato, and Beyer for at least the reasons described above with reference to claim 1.

In light of the above, Applicants respectfully request withdrawal of these rejections under 35 U.S.C. § 103(a).

III. Response to the Rejections under 35 U.S.C. § 103(a) Based on Librizzi/Shirato/Hirabayashi

The Examiner rejected claims 18 and 19 under 35 U.S.C. § 103(a) as being obvious in view of the combination of Librizzi, Shirato, and U.S. Patent No. 5,889,314 ("Hirabayashi"). Claims 18 and 19 depend from claim 1. As described above, neither Librizzi nor Shirato show or suggest a guard ring that extends through the buried insulation layer directly over the semiconductor substrate. The Examiner cited to Hirabayashi for the teaching of a semiconductor device that has a metal guard ring. (Office Action, page 4.) However, this teaching of Hirabayashi does not overcome the deficiencies identified with respect to Librizzi and Shirato. Accordingly, Applicants submit that claims 18 and 19 are not obvious in light of the combination of Librizzi, Shirato, and Hirabayashi for at least the reasons described above with reference to claim 1.

In light of the above, Applicants respectfully request withdrawal of these rejections under 35 U.S.C. § 103(a).

CONCLUSION

In light of the above remarks, Applicants submit that the present application is in condition for allowance and respectfully request notice to this effect. The Examiner is requested to contact Applicants' representative below if any questions arise or she may be of assistance to the Examiner.

Respectfully submitted,

Date: May 11, 2007

By: 

Lisa M. Schoedel
Reg. No. 53,564
McDonnell Boehnen Hulbert & Berghoff LLP
300 South Wacker Drive
Chicago, Illinois 60606-6709
312 935 2362
schoedel@mbhb.com